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EXAMINER	
THAMMAVONG, PRASITH	
ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application **or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,792	HSU, WENCHI	
	Examiner	Art Unit	
	Prasith Thammavong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/711,792 has a total of 42 claims pending in the application, there are 4 independent claims and 38 dependent claims, all of which are ready for examination by the examiner.

1. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is not found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**. The applicant's name does not match the applicant's signature in the Oath/Declaration.

2. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on an application 60/485,475 filed on 10/07/2003.

3. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC ' 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility.

With respect to claim 1-6, claim 1 provides a tangible result if all steps of the claim are accomplished. However, the conditional statement of "when a pre-fetching is activated" in the *pre-fetching* step provides an alternative where this step is not done;

and the conditional statement of "when a cache hit occurs" in the *adding* step provides an alternative where this step is not done; and the conditional statement of "when the counter value is smaller than the first threshold value" in the *when* step provides an alternative where this step is not done. If the *prefetching, adding, and when* steps do not occur, this claim would only recite the *initializing* step and *comparing* step. Therefore under this condition, there is no tangible result from the claim. **Claims 2-6** inherit the deficiencies of claim 1 since they depend on claim 1, and do not add any limitations provide a tangible result.

With respect to claim 7-12, claim 7 provides a tangible result if all steps of the claim are accomplished. However, the conditional statement of "when a pre-fetching is activated" in the *pre-fetching* step provides an alternative where this step is not done; and the conditional statement of "when a cache hit occurs" in the *adding* step provides an alternative where this step is not done; and the conditional statement of "when the counter value is larger than the first threshold value" in the *when* step provides an alternative where this step is not done. If the *prefetching, adding, and when* steps do not occur, this claim would only recite the *initializing* step and *comparing* step. Therefore under this condition, there is no tangible result from the claim. **Claims 8-12** inherit the deficiencies of claim 7 since they depend on claim 7, and do not add any limitations that provide a tangible result.

Claim Rejections - 35 USC ' 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 26 and 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 26 recites the limitation "the fourth threshold value" in lines 1 and 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the fourth threshold value” as “the fourth value.”

Claim 26 recites the limitation "the third threshold value" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the third threshold value” as “the third value.”

Claim 39 recites the limitation "the fourth threshold value" in lines 4 and 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the fourth threshold value” as “the fourth value.”

Claim 39 recites the limitation "the third threshold value" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the third threshold value” as “the third value.”

Claim 40 recites the limitation "the fourth threshold value" in lines 1 and 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the fourth threshold value” as “the fourth value.”

Claim 40 recites the limitation "the third threshold value" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner has construed “the third threshold value” as “the third value.”

6. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 13-17, 21-23, 27-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Kadi (US PGPUB # 2004/0117556 A1).

With respect to claim 1, the Kadi reference teaches a method for pre-fetching data from a memory, comprising the steps of:

initializing a counter value; (paragraph 33, the “threshold value”)

pre-fetching a predetermined data from the memory and subtracting a first value from the counter value when a pre-fetching is activated; (paragraph 33, where when prefetching occurs and when there is a miss, there is a decrement)

adding a second value to the counter value when a cache hit occurs; (paragraph 33, where when there is a hit, there is a increment)

comparing the counter value with a first threshold value; (paragraph 20, where the threshold value is compared to the number of the MP bits)

and when the counter value is smaller than the first threshold value, stopping pre-fetching data from the memory. (paragraph 19, where prefetching is not performed if the threshold value is greater than the number of the MP bits)

With respect to claim 2, the Kadi reference teaches when the pre-fetching is stopped, the counter value is blocked from being decreased by the first value. (paragraph 32, where the prefetching is off, and there are no outstanding transactions)

With respect to claim 3, the Kadi reference teaches when the pre-fetching is stopped and the cache hit occurs, the second value is added to the counter value (paragraph 32, where there could be outstanding transactions that could cause increments)

With respect to claim 6, the Kadi reference teaches the second value is an integer multiple of the first value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1).

With respect to claim 13, the Kadi reference teaches a pre-fetch controller for pre-fetching data from a memory for a logic operation unit, the pre-fetching controller comprising:

a register for storing a counter value; (paragraph 31, where the threshold value is stored in a register) and

a controller (paragraphs 32 and 33, the "third logic" and "first logic") electrically connected to the register for changing the counter value when a pre-fetching is activated or when a cache hit occurs. (paragraph 33, where the third logic increments/decrements the threshold value)

With respect to claim 14, the Kadi reference teaches the controller further comprises an operating unit for predicting a predetermined data required by the logic operation unit and pre-fetching the predetermined data from the memory when the pre-fetching is activated (paragraph 28, where the first logic checks if the data is in the prefetch buffer).

With respect to claim 15, the Kadi reference teaches the controller further comprises an output unit for decreasing the counter value by a first value when the pre-fetching is activated (paragraph 33, where when the threshold value is decremented for a miss).

With respect to claim 16, the Kadi reference teaches the controller further comprises a detecting unit for adding a second value to the counter value when the cache hit occurs (paragraph 33, where when the threshold value is incremented for a hit).

With respect to claim 17, the Kadi reference teaches the second value is an integer multiple of the first value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1).

With respect to claim 21, the Kadi reference teaches the controller further comprises an output unit for adding a third value to the counter value when the pre-fetching is activated. (paragraph 33, where the threshold value is incremented)

With respect to claim 22, the Kadi reference teaches the controller further comprises a detecting unit for subtracting a fourth value from the counter value when the cache hit occurs. (paragraph 33, where the threshold value is decremented)

With respect to claim 23, the Kadi reference teaches the fourth value is an integer multiple of the third value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1).

With respect to claim 27, the Kadi reference teaches teaches the pre-fetch controller further comprises a subtractor electrically connected to the register for changing the counter value. (paragraph 33, where the threshold value is decremented)

With respect to claim 28, the Kadi reference teaches the pre-fetch controller further comprises an adder electrically connected to the register for changing the counter value. (paragraph 33, where the threshold value is incremented)

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious

at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Kadi (US PGPUB # 2004/0117556 A1) in view of Kadowaki (US Patent # 6,654,873).

With respect to claim 4, the Kadi reference does not teach when the pre-fetching is stopped and the counter value is larger than a second threshold value, pre-fetching data from the memory is restarted.

However, the Kadowaki reference does teach when the pre-fetching is stopped and the counter value is larger than a second threshold value, pre-fetching data from the memory is restarted. (column 4, lines 62-65, where the prefetching is restarted from a suspended state)

The Kadi and Kadowaki references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference when the pre-fetching is stopped and the counter value is larger than a second threshold value, pre-fetching data from the memory is restarted, which is taught by the Kadowaki reference.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of faster operations to obtain the invention as specified in claim 4.

With respect to claim 18, the Kadi reference teaches the pre-fetch controller further comprises a comparing module electrically connected between the register and the controller for stopping pre-fetching data from the memory when the counter value becomes smaller than a first threshold value (paragraph 19, where the prefetching is stopped when the threshold value is less than the number of MP bits)

However, the Kadi reference does not teach restarting pre-fetching data from the memory when the counter value becomes larger than a second threshold value after the pre-fetching is stopped.

The Kadowaki reference teaches restarting pre-fetching data from the memory when the counter value becomes larger than a second threshold value after the pre-fetching is stopped (column 4, lines 62-65, where the prefetching is restarted from a suspended state).

The Kadi and Kadowaki references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference to restart pre-fetching data from the memory when the counter value becomes larger than a second threshold value after the pre-fetching is stopped, which is taught by the Kadowaki reference.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of faster operations to obtain the invention

as specified in claim 18.

With respect to claim 19, the Kadi reference teaches the counter value is blocked from being decreased by the first value when the pre-fetching is stopped (paragraph 32, where the prefetching is off, and there are no outstanding transactions), and the second value is added to the counter value when the pre-fetching is stopped and the cache hit occurs. (paragraph 32, where there could be outstanding transactions that could cause an increment).

Claims 7-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Kadi (US PGPUB # 2004/0117556 A1) in view of Steely (US Patent # 5,038,278).

With respect to claim 7, the Kadi reference teaches a method for pre-fetching data from a memory, comprising the steps of:

initializing a counter value; (paragraph 33, the "threshold value") and

comparing the counter value with a first threshold value; (paragraph 20, where the threshold value is compared to the number of the MP bits).

However, the Kadi reference does not explicitly teach:

subtracting a second value from the counter value when a cache hit occurs;

pre-fetching a predetermined data from the memory and adding a first value to the counter value when a pre-fetching is activated;

when the counter value is larger than the first threshold value, stopping pre-fetching data from the memory.

The Steely reference does teach implementing a counter to decrement when there is a hit versus to increment when there is a hit (column 4, lines 20-22). Therefore the combination of the Kadi and Steely references teach:

subtracting a second value from the counter value when a cache hit occurs; (Kadi, paragraph 33, where when there is a hit, there is a increment, [which could be substituted with a decrement as suggested by the Steely reference])

pre-fetching a predetermined data from the memory and adding a first value to the counter value when a pre-fetching is activated; (Kadi, paragraph 33, where when prefetching occurs and when there is a miss, there is a decrement [which could be substituted with a increment as suggested by the Steely reference])

when the counter value is larger than the first threshold value, stopping pre-fetching data from the memory. (Kadi, paragraph 19, where prefetching is not performed if the threshold value is less than [which could be substituted with greater than as suggested by the Steely reference] the number of the MP bits)

The Kadi and Steely references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference to:

subtracting a second value from the counter value when a cache hit occurs;

pre-fetching a predetermined data from the memory and adding a first value to the counter value when a pre-fetching is activated; and

when the counter value is larger than the first threshold value, stopping pre-fetching data from the memory, which is taught by the combination of Kadi and Steely references.

The suggestion/motivation for doing so would have been to increase flexibility of the type of counter to use (Steely, column 4, lines 9-23).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of flexibily to obtain the invention as specified in claim 7.

With respect to claim 8, the Kadi reference teaches the pre-fetching is stopped, the counter value is blocked from being increased by the first value. (paragraph 32, where the prefetching is off, and there are no outstanding transactions)

With respect to claim 9 the Kadi reference teaches when the pre-fetching is stopped and the cache hit occurs, the counter value is decreased by the second value (paragraph 32, where there could be outstanding transactions that could cause increments [which could be a decrement as suggested by the Steely reference]).

With respect to claim 12, the Kadi reference teaches the second value is an integer multiple of the first value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1)

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kadi (US PGPUB # 2004/0117556 A1) and Steely et al. (US Patent # 5,038,278) as applied to claim 9 above, and further in view of Kadowaki (US Patent # 6,654,873).

With respect to claim 10, the combination of the Kadi and Steely references does not teach when the pre-fetching is stopped and the counter value is smaller than a second threshold value, pre-fetching data from the memory is restarted.

However, the Kadowaki reference does teach when the pre-fetching is stopped and the counter value is smaller than a second threshold value, pre-fetching data from the memory is restarted. (column 4, lines 62-65, where the prefetching is restarted from a suspended state)

The Kadi, Steely, and Kadowaki references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Kadi and Steely references when the pre-fetching is stopped and the counter value is smaller than a second threshold value, pre-fetching data from the memory is restarted, which is taught by the Kadowaki reference.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of faster operations to obtain the invention as specified in claim 10.

Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadi (US PGPUB # 2004/0117556 A1) in view of Steely et al. (US Patent # 5,038,278) and Kadowaki (US Patent # 6,654,873).

With respect to claim 24, the Kadi reference does not explicity teach the pre-fetch controller further comprises a comparing module electrically connected between the register and the controller for stopping pre-fetching data from the memory when the counter value becomes larger than a third threshold value and for restarting pre-fetching data from the memory when the counter value becomes smaller than a fourth threshold value after the pre-fetching is stopped.

The Steely reference does teach implementing a counter to decrement when there is a hit versus to increment when there is a hit (column 4, lines 20-22). Therefore the combination of the Kadi and Steely references teach:

the pre-fetch controller further comprises a comparing module electrically connected between the register and the controller for stopping pre-fetching data from the memory when the counter value becomes larger than a third threshold value (Kadi, paragraph 19, where prefetching is not performed if the threshold value is less than [which could be substituted with greater than as suggested by the Steely reference] the number of the MP bits).

The Kadi and Steely references are analogous art because they are in the same field of endeavor of memory access and control.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference for the pre-fetch controller further to comprise a comparing module electrically connected between the register and the controller for

stopping pre-fetching data from the memory when the counter value becomes larger than a third threshold value.

However, the above combination of the Kadi and Steely reference does not explicitly teach restarting pre-fetching data from the memory when the counter value becomes smaller than a fourth threshold value after the pre-fetching is stopped.

The Kadowaki reference does teach restarting pre-fetching data from the memory when the counter value becomes smaller than a fourth threshold value after the pre-fetching is stopped. (Kadowaki, column 4, lines 62-65, where the prefetching is restarted from a suspended state).

The Kadi, Steely and Kadowaki references are analogous art because they are in the same field of endeavor of memory access and control.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of the combination of the Kadi and Steely references with the teachings of the Kadowaki reference for the benefit of increased prefetching to obtain the invention as specified in claim 24.

With respect to claim 25, the Kadi reference teaches the third value is blocked from being added to the counter value when the pre-fetching is stopped (paragraph 32, where the prefetching is off, and there are no outstanding transactions), and the fourth value is subtracted from the counter value when the pre-fetching is stopped and the

cache hit occurs. (paragraph 32, where there could be outstanding transactions that could cause an decrement).

Claim 29-35, 37-38, and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Kadi (US PGPUB # 2004/0117556 A1) in view of Kadowaki (US Patent # 6,654,873).

With respect to claim 29, the Kadi reference teaches a data processing device for pre-fetching data from a memory and providing data to a logic operation unit, the data processing device comprising:

a first memory for storing prediction data; (paragraph 28, the "prefetch buffer")

a second memory for storing data and providing the logic operation unit with data; (paragraph 28, the "data buffer")

a memory controller (paragraph 27, the "memory controller") electrically connected to the second memory for pre-fetching data from the second memory to the first memory; (paragraph 27, where the data is transferred from one memory to another) and

a pre-fetch controller (paragraph 32 and 33, the "first logic" and the third logic"), electrically connected between the second memory and the memory controller, for predicting a data required by the logic operating unit and controlling the memory controller to pre-fetch the data from the second memory, (paragraph 32, where the first logic determines which next cache line to get; and paragraph 33, where the third logic checks whether the requested data is in the prefetch buffer)

wherein the pre-fetch controller has a counter value (paragraph 33, the "threshold value") , compares the counter value with a first threshold value (paragraph 19, the "number of MP bits") to determine whether to stop a pre-fetching for data in the second memory (paragraph 19, where the comparison of the threshold value and number of MP bits determines on whether a prefetch is performed)

However, the Kadi reference does not teach comparing the counter value with a second threshold value to determine whether to restart pre-fetching data from the second memory after the pre-fetching is stopped.

The Kadowaki reference teaches comparing the counter value with a second threshold value to determine whether to restart pre-fetching data from the second memory after the pre-fetching is stopped (column 4, lines 62-65, where the prefetching is restarted from a suspended state).

The Kadi and Kadowaki references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference to compare the counter value with a second threshold value to determine whether to restart pre-fetching data from the second memory after the pre-fetching is stopped, which is taught by the Kadowaki reference.

The suggestion/motivation for doing so would have been to increase processor efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of faster operations to obtain the invention

as specified in claim 29.

With respect to claim 30, the Kadi reference teaches the pre-fetching controller comprises:

a register for storing the counter value; (paragraph 31, where the threshold value is stored in a register).

and a comparing module electrically connected to the register for comparing the counter value with a first threshold value and a second threshold value. (paragraph 19, where the threshold value is compared to the number of MP bits)

With respect to claim 31, the Kadi reference teaches the pre-fetching controller further comprises a controller electrically connected to the comparing module for changing the counter value when the pre-fetching is activated and the cache hit occurs (paragraph 33, where the prefetching takes place and there is an increment when the requested data in the prefetch buffer).

With respect to claim 32, the Kadi reference teaches the controller comprises: an operating unit for predicting the data required by the logic operating unit and controlling the memory controller to fetch the data from the second memory; an output unit for sending a first command when the pre-fetching is activated; and a detecting unit for sending a second command when the cache hit occurs. (paragraph 28, where the data is forwarded to the data buffer; and paragraph 33, where the prefetching takes place and there is an increment/decrement when the requested data is in the prefetch buffer)

With respect to claim 33, the Kadi reference teaches the counter value is decreased by a first value when the pre-fetching is performed, and the counter value is increased by a second value when the cache hit occurs. (paragraph 33, where when prefetching takes place, there is a decrement when there is a miss and an increment when there is a hit)

With respect to claim 34, the Kadi reference teaches the the second value is an integer multiple of the first value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1).

With respect to claim 35, the Kadi reference does not teach pre-fetching is stopped when the counter value becomes smaller than the first threshold value, and the pre-fetching is restarted when the counter value becomes larger than the second threshold value.

However, the Kadowaki reference does teach pre-fetching is stopped when the counter value becomes smaller than the first threshold value, and the pre-fetching is restarted when the counter value becomes larger than the second threshold value. (column 4, lines 62-65, where the prefetching is restarted from a suspended state)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kadi reference to have the pre-fetching to be stopped when the counter value becomes smaller than the first threshold value, and the pre-fetching is restarted when the counter value becomes larger than the second threshold value, which is taught by the Kadowaki reference.

The suggestion/motivation for doing so would have been to increase processor

efficiency (Kadowaki, column 1, line 63 to column 2, line 3).

Therefore it would have been obvious to combine the teachings of Kadi reference with the Kadowaki reference for the benefit of faster operations to obtain the invention as specified in claim 35.

With respect to claim 37, the Kadi reference teaches a third value is added to the counter value when the pre-fetching is activated, and a fourth value is subtracted from the counter value when the cache hit occurs. (paragraph 33, where threshold value is incremented/decremented)

With respect to claim 38, the Kadi reference teaches the fourth value is an integer multiple of the third value. (paragraph 33, where the decrement value is an integer multiple of the increment value, i.e. 1 x 1 = 1).

With respect to claim 41, the Kadi reference teaches the data processing device further comprises an adder electrically connected to the register for increasing the counter value. (paragraph 33, where the threshold value is incremented)

With respect to claim 42, the Kadi reference teaches the data processing device further comprises a subtractor electrically connected to the register for decreasing the counter value by a first value or a second value. (paragraph 33, where the threshold value is decremented)

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kadi (US PGPUB # 2004/0117556 A1) and Kadowaki (US Patent # 6,654,873) as applied to claim 37 above, and further in view of Steely et al. (US Patent # 5,038,278).

With respect to claim 39, the combination of the Kadi and Kadowaki references does not explicitly teach pre-fetching data from the second memory is stopped when the counter value becomes larger than the third threshold value, and pre-fetching data from the second memory is restarted when the counter value becomes smaller than the fourth threshold value.

The Steely reference does teach implementing a counter to decrement when there is a hit versus to increment when there is a hit (column 4, lines 20-22). Therefore the combination of the Kadi, Kadowaki and Steely references teach:

pre-fetching data from the second memory is stopped when the counter value becomes larger than the third threshold value (Kadi, paragraph 19; where prefetching is not performed if the threshold value is less than [which could be substituted with greater than as suggested by the Steely reference] the number of the MP bits), and

pre-fetching data from the second memory is restarted when the counter value becomes smaller than the fourth threshold value (Kadowaki, column 4, lines 62-65, where the prefetching is restarted from a suspended state).

The Kadi, Kadowaki and Steely references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Kadi and Kadowaki references to:

pre-fetching data from the second memory is stopped when the counter value becomes larger than the third threshold value, and

pre-fetching data from the second memory is restarted when the counter value becomes smaller than the fourth threshold value.

The suggestion/motivation for doing so would have been to increase flexibility of the type of counter to use. (Steely, column 4, lines 9-23)

Therefore it would have been obvious to combine the teachings of the combination of the Kadi and Kadowaki references with the teachings of the Steely reference for the benefit of flexibily to obtain the invention as specified in claim 39.

Claims 5, 20 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kadi (US PGPUB # 2004/0117556 A1) and Kadowaki (US Patent # 6,654,873) as applied to claims 4, 18 and 35 above, and further in view of the Examiner's taking of Official Notice.

With respect to claims 5, 20, and 36, the combination of the Kadi and Kadowaki references does not explicitly teach the second threshold value is larger than the first threshold value. However, the Kadi reference does teach that the number of MP bits is dynamic (paragraph 20). Therefore it was well known in the art at the time of the invention to have the second threshold value to be larger than the first threshold value and such Official Notice is taken. It would have been obvious to one of ordinary skill in the art to modify the Kadi and Kadowaki references to expand its teaching to have the second threshold value to be larger than the first threshold value in order to increase performance by allowing more prefetching and to decrease power consumption by reduce prefetching when additional prefetching is not needed, which is taught by the Kadi reference (paragraph 21).

Claims 11 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kadi (US PGPUB # 2004/0117556 A1), Kadowaki (US Patent # 6,654,873) and Steely et al. (US Patent # 5,038,278) as applied to claim 10 and 39 above, and further in view of the Examiner's taking of Official Notice.

With respect to claim 11 and 40, the combination of the Kadi, Steely and Kadowaki references does not explicitly teach the second threshold value is smaller than the first threshold value. However, the Kadi reference does teach that the number of MP bits is dynamic (paragraph 20). Therefore it was well known in the art at the time of the invention to have the second threshold value to be smaller than the first threshold value and such Official Notice is taken. It would have been obvious to one of ordinary skill in the art to modify the combination of the Kadi, Steely and Kadowaki references to expand its teaching to have the second threshold value to be smaller than the first threshold value in order to increase performance by allowing more prefetching and to decrease power consumption by reduce prefetching when additional prefetching is not needed, which is taught by the Kadi reference (paragraph 21).

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kadi (US PGPUB # 2004/0117556 A1) in view of the Examiner's taking of Official Notice.

With respect to claim 26, the combination of the Kadi reference does not explicitly teach the fourth threshold value is smaller than the third threshold value. However, the Kadi reference does teach that the number of MP bits is dynamic (paragraph 20). Therefore it was well known in the art at the time of the invention to

have the fourth threshold value to be larger than the third threshold value and such Official Notice is taken. It would have been obvious to one of ordinary skill in the art to modify the Kadi reference to expand its teaching to have the fourth threshold value to be smaller than the third threshold value in order to increase performance by allowing more prefetching and to decrease power consumption by reduce prefetching when additional prefetching is not needed, which is taught by the Kadi reference (paragraph 21).

4. RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

Mittel at al. (US Patent # 5,719,800), which teaches performance throttling to reduce IC power consumption.

5. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-42 have received a first action on the merits

and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasith Thammavong whose telephone number is (571) 270-1040 can normally be reached on Monday - Thursday 9:00am - 6:00pm and the first Friday of the bi-week, 9:00 am –5:00 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PT

Prasith Thammavong
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Art Unit 2187
December 27, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER